# In-Pixel Storage Techniques for CMOS Burst-Mode Ultra-High-Speed Imagers

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## ABSTRACT

This work presents in-pixel circuit techniques for burst-mode ultra-high-speed imagers to improve the noise performance while maintaining a dense analog memory storage for each pixel. Together with an AC coupling CDS stage, in-pixel amplification is demonstrated to be useful to improve effective frame depth for longer recording time. Considering the benefits on scaling and power consumption, a 108-cell memory bank (10fF/cell) is implemented inside the pixel. Two types of pixel variations were fabricated in CMOS 130nm technology. The photon transfer curves of both pixel types are measured over different operation speeds up to 20Mfps showing noise performance of both variations to be less than 10e- noise.

## INTRODUCTION

In order to achieve million fps with large image formats, burst-mode ultra-high-speed (e.g. 20Mfps) image sensors store a number of images inside the pixel (e.g. up to a few hundred frames) at high burst rate, and read these out at lower rate (e.g. 1000fps). Typically, CCD [1] or special CCD in CMOS [2] technology is used to store and read the packages of collected charge of all these images. Using CMOS technology (for its advantages of integration, cost, speed and power efficiency[3 - 5]), images stored in the voltage domain on very small capacitors (e.g. <10fF) generate very large kTC noise. More so, only a limited number of frames can be stored in the available area.

Without 3D stacking, the memory bank needs to be placed on the same chip. In [3,5], the memory bank is placed outside the pixel array, which gives higher design freedom on both photo-sensitive as well as the non-photo-sensitive area, such as better light shielding in the memory part. In this work, a local storage architecture is chosen based on two reasons. Firstly, no functionality needs to be shared between pixels, which allows for simpler upscaling of the array size. Secondly, a short signal path means there is no need to drive a long high capacitance line over the whole pixel array at high speed, bringing down the power consumption.

Due to the existence of the analog memory bank, which usually requires several buffering stages, higher gain along the readout chain is more desirable [3]. The additional amplification before the storage of the signal will not only suppress the kTC noise from the small analog memory but also relax the noise requirements for the following blocks. Constrained by the global shutter requirement, such an amplification block must be implemented at the pixel level. Therefore, the design challenge is to implement the amplifier in a small area with low power consumption. The resulting low fill factor can be addressed by using back-side illumination (BSI) technology.

## IMPLEMENTATION

The prototype image sensor is shown in Fig. 1. Besides the pixel array, the chip is composed of a row driver, a column driver and an analog readout block. Additionally, a network on chip (NoC) is placed for the chip configuration. The pixel array is made of two pixel variations, each has 32 × 84 pixels. After the burst capturing, the pixel output voltages are passed on row-wise via the analog sampling stage. Each column signal is read out slowly by off-chip ADCs through the mux and analog buffers.

The generic pixel topology is depicted in Fig. 2. It includes 3 blocks: the photo-sensitive core (4T structure is used), the CDS amplification and the memory bank. An AC coupling capacitor is used to perform in-pixel CDS to reduce the number of required data storage by two, as opposed to sampling both reset and video signals [3]. Secondly, limited by the signal swing of following readout block, a small amplification gain will be efficient to improve the noise performance [6]. With the single transistor passive amplification [7], the weak pixel signal is amplified prior to the storing to suppress the kTC noise of the small storage capacitors. The detailed implementations of two different flavors are shown in Fig. 3, featuring NMOS only circuitry.

Both amplifiers take the same area of 5µm × 25µm. Besides the additional source follower (SF) stage, $M_{SF}$ in the type B, all control signals remain the same. The memory bank structure and the layout of the pixel are shown in Fig. 4 and Fig. 5.

Although the AC coupling CDS stage introduces additional kTC noise, compared to kTC noise generated at the FD node and memory storage, the kTC noise from CDS operation is much smaller thanks to its much larger capacitance. Since a higher frame depth leads to lower capacitance memories, it suggests the AC coupling CDS technique is more suitable for high frame depth applications.

One limitation for type A is that the CDS stage inherently also serves as a capacitive voltage divider, which sets the gain by the ratio of the capacitances of $M_{CDS}$ and $M_{SAMP}$, $C_{CDS}/(C_{CDS} + C_{SAMP})$. Thus, it will be very difficult to achieve a gain close to one. In this design, $C_{CDS}$ is sized at 4 times bigger than $C_{SAMP}$ to reach the gain of 0.8 keeping a good balance between area and gain loss. Compared to type A, the extra SF stage is inserted in type B breaking the capacitive division in the CDS stage. The CDS stage gain is therefore mainly defined by the SF gain, which is usually slightly lower than 1 with the body effect. It allows the use of a smaller CDS capacitor $M_{CDS}$ and a larger storage capacitor $M_{SAMP}$, which can improve the gain during passive amplification since the impact of parasitic capacitance will be less pronounced.

## OPERATIONS

The CDS operation starts with resetting the FD node via $M_1$. The voltages over $M_{CDS}$ and $M_{SAMP}$ are reset by keeping switch R, S and INV closed. Secondly, when RST goes low, R is turned off shortly after the clock feedthrough settles. Thus, the FD reset voltage including the kTC noise $V_{N,FD}$ is buffered via the SF $M_2$ and sampled over $M_{CDS}$ against $V_{PRE}$. Later, with the TX gate on, the charge is integrated at the FD node, then any further voltage drop will pass through $M_{CDS}$ as AC coupling signal. Thus, the video signal will be only be referred to the fixed voltage $V_{PRE}$ without the presence of $V_{N,FD}$. The CDS operation is completed by switching S off, when the video signal is sampled respect to the ground. In type B, the signal is buffered via SF $M_{SF}$.

The amplification operation follows immediately by toggling the voltage on the shorted source and drain of $M_{SAMP}$ from ground to a DC voltage $V_{DEP}$. The gain is realized by taking advantage of the intrinsic characteristic of the MOS transistor: when the transistor is biased in inversion, the capacitance value of $C_{SAMP,\ INV}$ can be several times larger compared to $C_{SAMP,\ DEP}$ in the depletion region. Due to charge conservation on $M_{SAMP}$, the voltage gain will simply be defined as $C_{SAMP,INV}/C_{SAMP,DEP}$. With the presence of parasitic capacitances, which dilutes the maximum gain, a gain of about 3X can be realized. Finally, the signal is stored on one analog memory out of 108 memory cells.

## MEASUREMENT RESULTS

Despite the fact that a 4T pixel core has been used which was not optimized for speed, the photon transfer curve (PTC) measurements have been evaluated over different burst frame rates confirming the viability of both proposed circuitries. Both pixel types are only consuming 10µA/pixel with 3.3V supply voltage, despite the different operation speeds. PTC measurements for both pixel types are shown in Fig. 6. The 20Mfps cases of both variations show the FD node referred read noise of less than 10e-, including the noise of the imager readout blocks (samplers, buffers and off-chip ADC). With the area budget, the benefits from the area reduction on the $M_{CDS}$ comes with the overhead cost of the extra SF stage. Therefore, the measured dynamic range of type B is 57dB, which is rather similar to 56dB of type A. Nevertheless, type B will be more suitable for larger pitch application. As expected, with the larger $M_{SAMP}$, the passive amplification in type B shows 30% higher gain. It confirms that the parasitic capacitance plays an important role in the single transistor passive amplification.

By delaying the trigger time of LED light pulse in each burst capture, a series of images at 5Mfps operation is obtained, which is shown in Fig. 8 demonstrating the functionality of the test imager. Table 1 is the test chip performance summary.

## CONCLUSTIONS

This work presents a low noise ultra-high speed burst-mode readout imager with two variations of in-pixel circuitries featuring the in-pixel storage techniques with NMOS-only in-pixel CDS and amplification. The measurement shows that 10e- low noise performance at 20Mfps can be reached with in-situ storage of 108 effective frames in 30µm pitch.

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## FIGURES AND TABLES

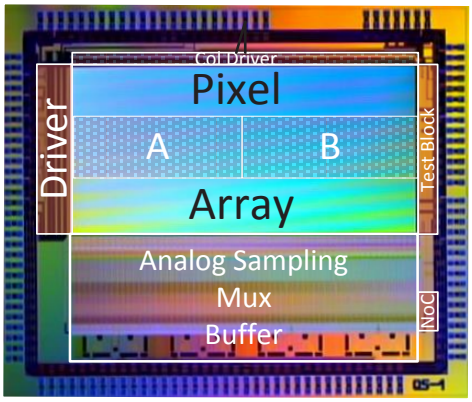


Figure 1– Image sensor micrograph indicating chip blocks and pixel locations

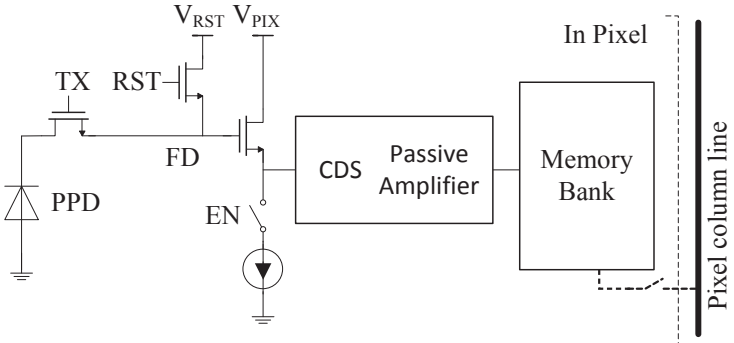


Figure 2 – Proposed in-pixel circuitry block diagram

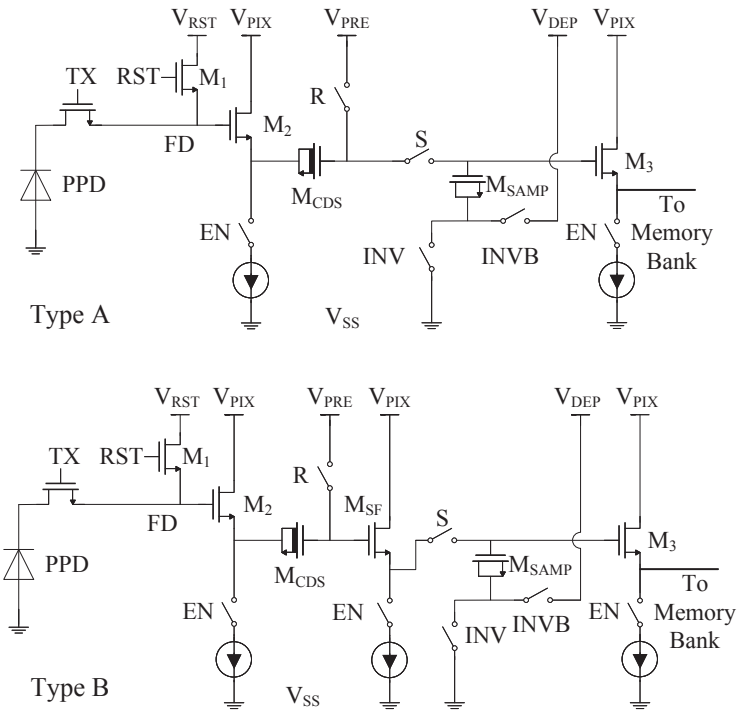


Figure 3 – Pixel type A and type B implementations

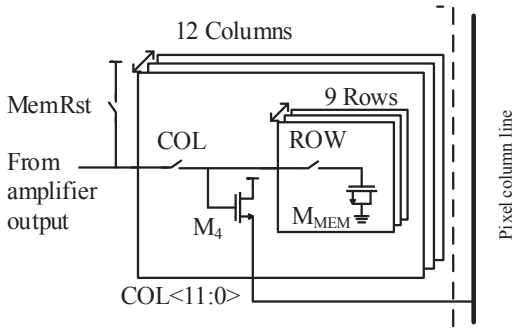


Figure 4– Memory bank implementation

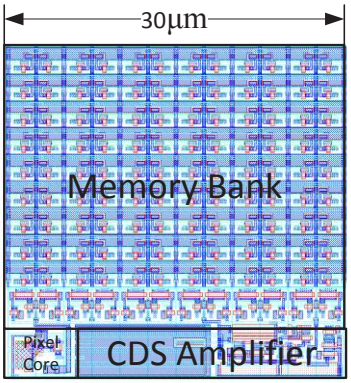


Figure 5 – Pixel layout (type A), each memory has capacitance of 10fF with the area of 2.5µm×2.4µm (including the logic switch).

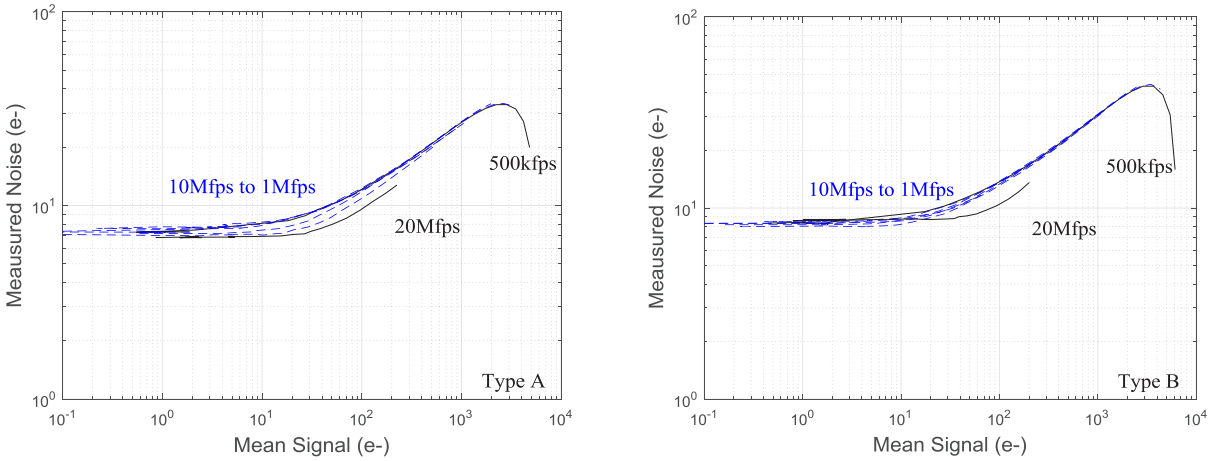


Figure 6 – PTCs have been measured over different burst frame rates for type A/B, respectively. Limited by LED illumination power, only PTC @ 500kfps is able to reach the full well capacity. PTC curves are well overlapping for different burst frame rates. The only exception is 20Mfps case, which needs further investigation.

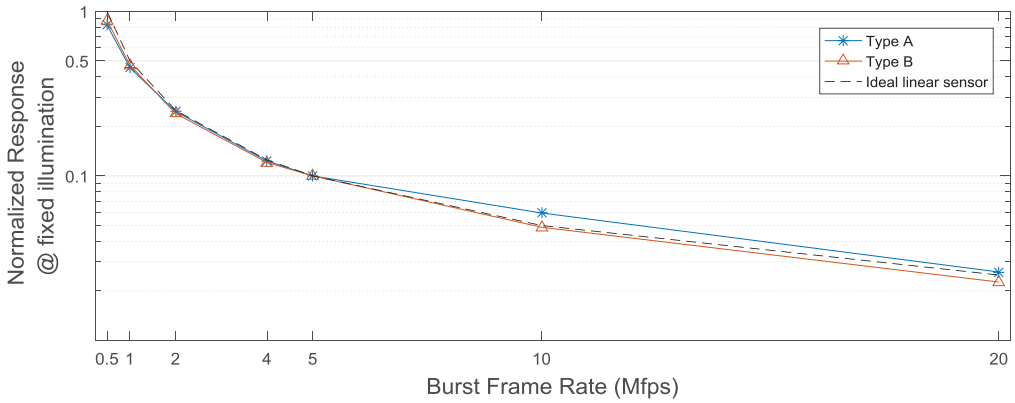


Figure 7 – With the fixed illumination, the output response is extracted against different operation speeds, to confirm the correct operation. Since Tint is inversely proportional to the burst frame rate, the output responses scale with burst frame rates as expected.

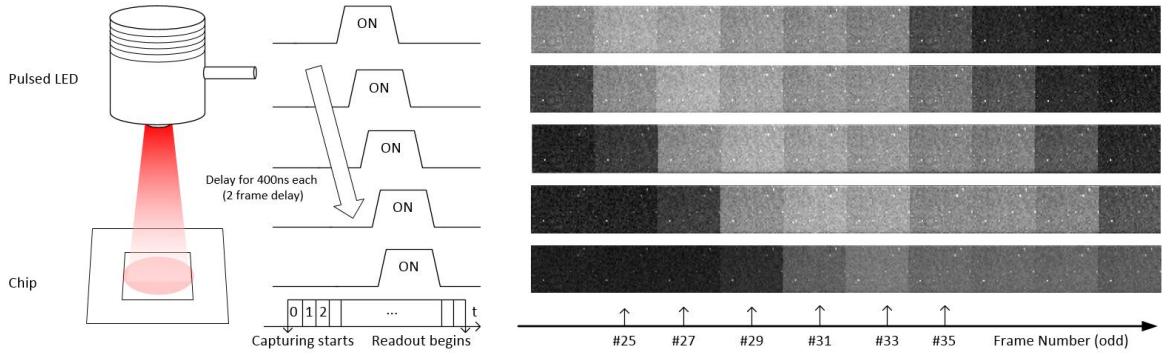


Figure 8 – Pictures taken with a pulsed LED illumination at 5Mfps (limited by illumination intensity)

Table 1 – Image sensor performance

| Technology | 130nm CMOS CIS | Burst rate | 20Mfps |
|---|---|---|---|
| Pixel Size | 30µm | Read noise | 9e- (type A)<br>8.4e- (type B) |
| Memory Depth | 108 (10fF/cell) | Dynamic Range (@500kfps) | 56 dB (type A)<br>57 dB (type B) |
| Pixel Size | 32×84 (same for type A/B) | Conversion Gain | 105µV/e- |
| Full Well Capacity | 6ke- | Power | 10µA/pixel @ 3.3V |